EAST SEARCH

9/18/04

L#	Hits	Search String	Databases
L1	6	6131078.uref.	USPAT; US-PGPUB; EPO; IBM_TDB
L2	7	5691925.uref.	USPAT; US-PGPUB; EPO; IBM_TDB
L3	0	trajectory near2 evaulation	USPAT; US-PGPUB; EPO; IBM_TDB
L4	13	pre-image and label and edge	USPAT; US-PGPUB; EPO; IBM_TDB
L5	95	edge and label and reachability	USPAT; US-PGPUB; EPO; IBM_TDB
L6	1	assertion adj graph	USPAT; US-PGPUB; EPO; IBM_TDB
L7	36	bdd and edge and label	USPAT; US-PGPUB; EPO; IBM_TDB

Results of search set L5:

US 20040172626 A1	Method for executing a sequential program in parallel with automatic fault tolerance	20040902	717/149
US 20040151180 A1	Enhanced H-VPLS service architecture using control word	20040805	370/392
US 20040093492 A1	Virtual private network management with certificates	20040513	713/156
US 20040088542 A1	Virtual private network crossovers based on certificates	20040506	713/156
US 20040088389 A1	Methods and apparatus for automated edge device configuration in a heterogeneous network	20040506	709/221
US 20040060007 A1	Efficient processing of XPath queries	20040325	715/513
US 20040054807 A1	System and method for creating improved overlay network with an efficient distributed data structure	20040318	709/243
US 20040049597 A1	SVC-L2.5 VPNs: combining Layer-3 VPNs technology with switched MPLS/IP L2VPNs for ethernet, ATM and frame relay circuits	20040311	709/242
US 20040039630 A1	Method and system for inferring and applying coordination patterns from individual work and communication activity	20040226	705/11
US 20040034702 A1	Method and apparatus for exchanging intra-domain routing information between VPN sites	20040219	709/224
US 20040032856 A1	Transparent, look-up-free packet forwarding method for optimizing global network throughput based on real-time route status	20040219	370/351
US 20030228147 A1	Technique for implementing a virtual private optical switched transport network using virtual private optical/TDM cross-connect technology	20031211	398/50
US 20030210695 A1	Method for forwarding data packets as cell sequences within a subnetwork of a data packet network	20031113	370/392
US 20030200307 A1	System and method for information object routing in computer networks	20031023	709/224
US 20030158720 A1	Space reduction in compositional state systems	20030821	703/17

US 20030154003 A1	Modeling reaction pathways	20030814	700/266
US 20030123457 A1	Apparatus and method for distributed software implementation of OSPF protocol	20030703	370/400
US 20030123446 A1	System for supply chain management of virtual private network services	20030703	370/392
US 20030118036 A1	Routing traffic in a communications network	20030626	370/401
US 20030117954 A1	Telecommunications system employing virtual service network architecture	20030626	370/230
US 20030110290 A1	Mobile tracking system for QoS guaranteed paths, router device used for this system, mobile communications terminal, and control program for controlling router device	20030612	709/242
US 20030101278 A1	System and method for directing clients to optimal servers in computer networks	20030529	709/240
US 20030076829 A1	Resource management in heterogenous QoS-based packet Networks	20030424	370/391
US 20030072270 A1	Method and system for topology construction and path identification in a two-level routing domain operated according to a simple link state routing protocol	20030417	370/254
US 20030059157 A1	Wavelength modulation for optical based switching and routing	20030327	385/24
US 20030043821 A1	Network-system, management-system, method and computer program product	20030306	370/400
US 20030041095 A1	Method and system for data transformation in a heterogeneous computer system	20030227	709/201
US 20030037041 A1	System for automatic determination of customized prices and promotions	20030220	707/1
US 20030033582 A1	Representations for estimating distance	20030213	716/4
US 20030031123 A1	Scalable configurable network of sparsely interconnected hyper-rings	20030213	370/216
US 20030014742 A1	Technique for compiling computer code to reduce energy consumption while executing the code	20030116	717/158
US 20030005145 A1	Network service assurance with comparison of flow activity captured outside of a service network with flow activity captured in or at an interface of a service network	20030102	709/238
US 20020181485 A1	APPARATUS AND METHOD FOR INTERNET PROTOCOL FLOW RING PROTECTION SWITCHING	20021205	370/419
US 20020178401 A1	Methods for enhancing program analysis	20021128	714/38
US 20020172157 A1	Method and system for fast computation of routes under multiple network states with communication continuation	20021121	370/238
US 20020116501 A1	Service tunnel over a connectionless network	20020822	709/227
US 20020105922 A1	Label switched packet transfer	20020808	370/328
US 20020087275 A1	Visualization and manipulation of biomolecular relationships using graph operators	20020704	702/19
US 20020075540 A1	Modular high capacity network	20020620	398/82
US 20020062463 A1	Dynamic control graphs for analysis of coordination-centric software designs	20020523	714/38
US 20020049838 A1	Liveexception system	20020425	709/224
US 20020044558 A1	Distributed IP over ATM architecture	20020418	370/395.52

US 20020024974 A1	Jitter reduction in Differentiated Services (DiffServ) networks	20020228	370/516
US 20020021675 A1	System and method for packet network configuration debugging and database	20020221	370/254
US 20020013934 A1	Formal verification of a logic design through implicit enumeration of strongly connected components	20020131	716/4
US 6760775 B1	System, method and apparatus for network service load and reliability management	20040706	709/238
US 6721269 B2	Apparatus and method for internet protocol flow ring protection switching	20040413	370/227
US 6711152 B1	Routing over large clouds	20040323	370/351
US 6651246 B1	Loop allocation for optimizing compilers	20031118	717/160
US 6621798 B1	Method to sequence changes for IP network configuration	20030916	370/256
US 6596701 B1	S-adenosyl methionine regulation of metabolic pathways and its use in diagnosis and therapy	20030722	514/46
US 6536018 B1	Reverse engineering of integrated circuits	20030318	716/4
US 6530079 B1	Method for optimizing locks in computer programs	20030304	717/158
US 6526551 B2	Formal verification of a logic design through implicit enumeration of strongly connected components	20030225	716/5
US 6526056 B1	Virtual private network employing tag-implemented egress-channel selection	20030225	370/392
US 6516306 B1	Model checking of message flow diagrams	20030204	706/10
US 6505342 B1	System and method for functional testing of distributed, component-based software	20030107	717/104
US 6493349 B1	Extended internet protocol virtual private network architectures	20021210	370/409
US 6490244 B1	Layer 3 routing in self-healing networks	20021203	370/216
US 6483833 B1	Method for transmitting label switching control information using the open shortest path first opaque link state advertisement option protocol	20021119	370/392
US 6463061 B1	Shared communications network employing virtual-private-network identifiers	20021008	370/392
US 6460036 B1	System and method for providing customized electronic newspapers and target advertisements	20021001	707/10
US 6427234 B1	System and method for performing selective dynamic compilation using run-time information	20020730	717/140
US 6421808 B1	Hardware design language for the design of integrated circuits	20020716	716/1
US 6381738 B1	Method for optimizing creation and destruction of objects in computer programs	20020430	717/140
US 6370685 B1	Data-flow method of analyzing definitions and uses of L values in programs	20020409	717/141
US 6351465 B1	System for routing packet switched traffic	20020226	370/395.43
US 6339595 B1	Peer-model support for virtual private networks with potentially overlapping addresses	20020115	370/392
US 6330614 B1	Internet and related networks, a method of and system for substitute use of checksum field space in information processing datagram headers for obviating processing speed and addressing space limitations and providing other features	20011211	709/236

US 6324496 B1	Model checking of hierarchical state machines	20011127	703/17
US 6295515 B1	Static partial order reduction	20010925	703/13
US 6237127 B1	Static timing analysis of digital electronic circuits using non-default constraints known as exceptions	20010522	716/6
US 6209120 B1	Verifying hardware in its software context and vice-versa	20010327	716/5
US 6205488 B1	Internet protocol virtual private network realization using multi-protocol label switching tunnels	20010320	709/238
US 6148000 A	Merging of data cells at network nodes	20001114	370/397
US 6130889 A	Determining and maintaining hop-count for switched networks	20001010	370/397
US 6077313 A	Type partitioned dataflow analyses	20000620	717/155
US 6069889 A	Aggregation of data flows on switched network paths	20000530	370/351
US 6055561 A	Mapping of routing traffic to switching networks	20000425	709/200
US 6029195 A	System for customized electronic identification of desirable objects	20000222	725/116
US 6009097 A	System for routing packet switched traffic	19991228	370/395.52
US 5937195 A	Global control flow treatment of predicated code	19990810	717/156
US 5867649 A	Dance/multitude concurrent computation	19990202	709/201
US 5835087 A	System for generation of object profiles for a system for customized electronic identification of desirable objects	19981110	345/810
US 5754939 A	System for generation of user profiles for a system for customized electronic identification of desirable objects	19980519	455/3.04
US 5754938 A	Pseudonymous server for system for customized electronic identification of desirable objects	19980519	725/116
US 5752241 A	Method and apparatus for estimating transitive closure and reachability	19980512	707/3
US 5710927 A	Method of replacing lvalues by variables in programs containing nested aggregates in an optimizing compiler	19980120	717/155
US 5680552 A	Gateway system for interconnecting different data communication networks	19971021	709/250
US 5659555 A	Method and apparatus for testing protocols	19970819	714/738
US 5615137 A	On-the-fly model checking with partial-order state space reduction	19970325	703/17
US 5574919 A	Method for thinning a protocol	19961112	712/220
US 5485409 A	Automated penetration analysis system and method	19960116	713/200
US 5327544 A	Method and apparatus for designing gateways for computer networks	19940705	716/18
US 5163016 A	Analytical development and verification of control-intensive systems	19921110	716/5

Results of search set L7:

US 20040078767 A1	Representing the design of a sub-module in a hierarchical integrated circuit design and analysis system	20040422	716/8
US 20030233622 A1	Method and apparatus for an asynchronous pulse logic circuit	20031218	716/1
US 20030224477 A1	Optimized promoter constructs	20031204	435/69.1
US 20030158720 A1	Space reduction in compositional state systems	20030821	703/17

US 20030154003 A1	Modeling reaction pathways	20030814	700/266
US 20030033126 A1	Modeling biological systems	20030213	703/11
US 20020178401 A1	Methods for enhancing program analysis	20021128	714/38
US 20020165701 A1	Method of configuring a product	20021107	703/7
US 20020078431 A1	Method for representing information in a highly compressed fashion	20020620	717/100
US 20020062463 A1	Dynamic control graphs for analysis of coordination-centric software designs	20020523	714/38
US 20020013934 A1	Formal verification of a logic design through implicit enumeration of strongly connected components	20020131	716/4
US 6732336 B2	Method and apparatus for an asynchronous pulse logic circuit	20040504	716/1
US 6587990 B1	Method and apparatus for formula area and delay minimization	20030701	716/2
US 6536018 B1	Reverse engineering of integrated circuits	20030318	716/4
US 6530063 B1	Method and apparatus for detecting equivalent and anti-equivalent pins	20030304	716/3
US 6526551 B2	Formal verification of a logic design through implicit enumeration of strongly connected components	20030225	716/5
US 6502232 B1	Electronic circuit design environmentally constrained test generation system	20021231	716/18
US 6466624 B1	Video decoder with bit stream based enhancements	20021015	375/240.27
US 6421808 B1	Hardware design language for the design of integrated circuits	20020716	716/1
US 6345379 B1	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	20020205	716/4
US 6334205 B1	Wavefront technology mapping	20011225	716/7
US 6295515 B1	Static partial order reduction	20010925	703/13
US 6247165 B1	System and process of extracting gate-level descriptions from simulation tables for formal verification	20010612	716/5
US 6185516 B1	Automata-theoretic verification of systems	20010206	703/2
US 6075932 A	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	20000613	716/4
US 5946475 A	Method for performing transistor-level static timing analysis of a logic circuit	19990831	716/6
US 5937183 A	Enhanced binary decision diagram-based functional simulation	19990810	703/14
US 5768498 A	Protocol verification using symbolic representations of queues	19980616	714/39
US 5696694 A	Method and apparatus for estimating internal power consumption of an electronic circuit represented as netlist	19971209	716/5
US 5696692 A	Conditional selection method for reducing power consumption in a circuit	19971209	716/1
US 5689435 A	Systems and methods for automated bracket design	19971118	703/1
US 5682519 A	Method for reducing power consumption of switching nodes in a circuit	19971028	716/2
US 5682320 A	Method for electronic memory management during estimation of average power consumption of an electronic circuit	19971028	716/4
US 5668732 A	Method for estimating power consumption of a cyclic sequential electronic circuit	19970916	702/60
US 5649166 A	Dominator selection method for reducing power consumption in a circuit	19970715	716/2
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Zames, G.;
Automatic Control, IEEE Transactions on , Volume: 11 Issue: 3 , Jul 1966
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[Abstract] [PDF Full-Text (1104 KB)] **IEEE JNL**

2 **Optimal parallel algorithm for the Hamiltonian cycle problem on dense graphs**
Dahlhaus, E.; Hajnal, P.; Karpinski, M.;
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3 **TYRO: a constraint based graphic designer's apprentice**
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Freeman-Benson, B.N.; Maloney, J.;
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5 **Verifying finite state real-time discrete event processes**
Ostroff, J.S.;
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6 **Distributed expertise: motivation to explore alternative approaches**
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8 **Performing logical database design using an E-R graph rewriting system**
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Wang, K.; Yuan, L.Y.;
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14 **The algorithmic aspects of the regularity lemma**
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73 **Surviving Java for mobiles**
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Pervasive Computing, IEEE , Volume: 2 Issue: 2 , April-June 2003
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[Abstract] [PDF Full-Text (573 KB)] **IEEE JNL**

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1 Formal verification of content addressable memories using symbolic trajectory evaluation

Manish Pandey, Richard Raimi, Randal E. Bryant, Magdy S. Abadir

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(136.65 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

In this paper we report on new techniques for verifying contentaddressable memories (CAMs), and demonstrate that these techniqueswork well for large industrial designs. It was shown in [Formal verification of PowerPC(TM) arrays using symbolic trajectory evaluation], that theformal verification technique of symbolic trajectory evaluation (STE)could be used successfully on memory arrays. We have extended thatwork to verify what are perhaps the most combinatorially difficultclass of memory arrays, ...

2 Linking BDD-based symbolic evaluation to interactive theorem-proving

Jeffrey J. Joyce, Carl-Johan H. Seger

July 1993 **Proceedings of the 30th international conference on Design automation**

Full text available: pdf(744.74 KB)

Additional Information: full citation, references, citings, index terms

3 Automatic generation of assertions for formal verification of PowerPC microprocessor arrays using symbolic trajectory evaluation

Li-C. Wang, Magdy S. Abadir, Nari Krishnamurthy

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(212.91 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

For verifying complex sequen tialbloc ks such as microprocessor embedded arrays, the formal method of symbolic trajectory ev aluation (STE) has achieved great success in the past [[3], [5], [6]]. P ast STE methodology for arrays requires manual creation of "assertions" to which both the RTL view and the actual design should be equivalent. In this paper, w e describe a novel method to automate the assertion creation process which improves the efficiency and the quality of array v ...

4 Formal verification of PowerPC arrays using symbolic trajectory evaluation

Manish Pandey, Richard Raimi, Derek L. Beatty, Randal E. Bryant

June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(122.46 KB) Additional Information: full citation, references, citings, index terms

5 GSTE through a case study

Jin Yang, Amit Goel

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(183.43 KB) Additional Information: full citation, abstract, references, citings, index terms

Generalized Symbolic Trajectory Evaluation (GSTE) [17, 18, 19] is a very significant extension of STE that has the power to verify all ω-regular properties but at the same time preserves the benefits of the original STE [16]. It also extends the symbolic quaternary model used by STE to support seamless model refinement for efficiency and accuracy trade-off in GSTE model checking. In this paper, we present a case study on FIFO verification to illustrate the strength of GSTE and demonstrate ...

6 Formal verification: A hybrid verification approach: getting deep into the design

Scott Hazelhurst, Osnat Weissberg, Gila Kamhi, Limor Fix

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(93.27 KB) Additional Information: full citation, abstract, references, index terms

One method of handling the computational complexity of the verification process is to combine the strengths of different approaches. We propose a hybrid verification technology combining symbolic trajectory evaluation with either symbolic model checking or SAT-based model checking. This reduces significantly the cost (both human and computing) of verifying circuits with complex initialisation, as well as simplifying proof development by enhancing verification productivity. The approach has been ...

Keywords: hybrid verification, symbolic model checking, symbolic trajectory evaluation

f

7 Formal verification in hardware design: a survey

Christoph Kern, Mark R. Greenstreet

April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2

Full text available: pdf(411.53 KB) Additional Information: full citation, abstract, references, citings, index terms

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

Keywords: case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

8 Real chalenges and solutions for validating system-on-chip: High level formal verification of next-generation microprocessors

Tom Schubert

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(249.00 KB) Additional Information: full citation, abstract, references, index terms

Formal property verification has been an effective complement to pre-silicon validation of several Intel Pentium 4 CPU designs at Intel Corporation. The principal objective of this program has been to prove design correctness rather than hunt for bugs. In the process, we have evolved our tools and methodology and are now applying FPV techniques to protocol level properties. Moving forward, new technologies such as GSTE and SAT offer the potential to significantly increase the scope of what can b ...

Keywords: formal property verification

9 On measuring the effectiveness of various design validation approaches for PowerPC microprocessor embedded arrays

Li-C. Wang, Magdy S. Abadir, Jing Zeng

October 1998 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 3 Issue 4

Full text available: pdf(258.15 KB) Additional Information: full citation, abstract, references, index terms

Design validation for embedded arrays remains as a challenging problem in today's microprocessor design environment. At Somerset, validation of array designs relies on both formal verification and vector simulation. Although several methods for array design validation have been proposed and had great success [Ganguly et al. 1996; Pandey et al. 1996, 1997; Wang and Abadir 1997], little evidence has been reported for the effectiveness of these methods with respect to the detection of design e ...

Keywords: ATPG, assertion test generation, design error model, logic verification, symbolic trajectory evaluation, validation

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10 Formal verification using parametric representations of Boolean constraints

Mark D. Aagaard, Robert B. Jones, Carl-Johan H. Serger

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(87.14 KB) Additional Information: full citation, references, citings, index terms

11 Low Power Design: Power and CAD considerations for the 1.75mbyte, 1.2ghz L2 cache on the alpha 21364 CPU

Joel Grodstein, Rachid Rayess, Tad Truex, Linda Shattuck, Sue Lowell, Dan Bailey, David Bertucci, Gabriel Bischoff, Daniel Dever, Mike Gowan, Roy Lane, Brian Lilly, Krishna Nagalla, Rahul Shah, Emily Shriver, Shi-Huang Yin, Shannon Morton

April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

Full text available: pdf(205.76 KB) Additional Information: full citation, abstract, references, index terms

A 1.75 MByte L2 cache has been designed and fabricated as part of the Alpha 21364 microprocessor[1] (Figure 1), in a .18m bulk CMOS process. The cache was designed to run at 1.2 GHz, and pass-1 samples confirm this. While Alpha CPUs are known primarily for high speed, the combination of package constraints and a tight schedule forced careful attention to the integrated whole of power expenditure and the interaction of CAD with design. The cache consumes only 7% of total die power.

Keywords: CPU, cache memory, logic verification, low-power, timing verification

12 Formal verification of iterative algorithms in microprocessors

Mark D. Aagaard, Robert B. Jones, Roope Kaivola, Katherine R. Kohatsu, Carl-Johan H. Seger

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(81.11 KB) Additional Information: full citation, abstract, references, citings, index terms

Contemporary microprocessors implement many iterative algorithms. For example, the front-end of a microprocessor repeatedly fetches and decodes instructions while updating internal state such as the program counter; floating-point circuits perform divide and square root computations iteratively. Iterative algorithms often have complex implementations because of performance optimizations like result speculation, re-timing and circuit redundancies. Verifying these iterative circuits a ...

13 Formal verification of a superscalar execution unit

Kyle L. Nelson, Alok Jain, Randal E. Bryant

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(290.81 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

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Many modern systems are designed as a set of interconnectedreactive subsystems. The subsystem verification task is toverify an implementation of the subsystem against the simple deterministichigh-level specification of the entire system. Our verificationmethodology, based on Symbolic Trajectory Evaluation, is ableto bridge the wide gap between the abstract specification and theimplementation specific details of the subsystem. This paper presentsa detailed description of an industrial application ...

14 Formal hardware verification by symbolic ternary trajectory evaluation

Randal E. Bryant, Derek L. Beatty, Carl-Johan H. Seger

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Full text available: pdf(613.01 KB) Additional Information: full citation, references, citings, index terms

15 Measuring the effectiveness of various design validation approaches for PowerPCTM microprocessor arrays

L.-C. Wang, M. S. Abadir, J. Zeng

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(200.86 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

Although several methods for array design validation have been proposed and had great success in the past, little evidence has been reported for the effectiveness of these methods with respect to the detection of design errors. In this paper, we propose a new way of measuring the effectiveness of different validation approaches based on automatic design error injection and simulation. This technique provides a systematic way for the evaluation of the quality of various validation approaches. Exp ...

Keywords: Design Error Models, Design Validation, Verification

16 Combining theorem proving and trajectory evaluation in an industrial environment

Mark D. Aagaard, Robert B. Jones, Carl-Johan H. Seger

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(149.69 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We describe the verification of the IM: a large, complex (12,000gates and 1100 latches) circuit that detects and marks the boundariesbetween Intel architecture (IA-32) instructions. We verified agate-level model of the IM against an implementation-independentspecification of IA-32 instruction lengths. We used theorem provingto to derive 56 model-checking runs and to verify that the model-checkingruns imply that the IM meets the specification for all possiblesequences of IA-32 instructions. Our v ...

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17 The formal verification of a pipelined double-precision IEEE floating-point multiplier

Mark D. Aagaard, Carl-Johan H. Seger

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(47.36 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Floating-point circuits are notoriously difficult to design and verify. For verification, simulation barely offers adequate coverage, conventional model-checking techniques are infeasible, and theorem-proving based verification is not sufficiently mature. In this paper we present the formal verification of a radix-eight, pipelined, IEEE double-precision floating-point multiplier. The verification was carried out using a mixture of model-checking and theorem-proving techniques in the Voss hardwar ...

Keywords: Hardware verification, floating-point arithmetic, ANSI/IEEE Std 754-1985, model checking, theorem proving

18 Advances in boolean analysis techniques: A SAT-based algorithm for reparameterization in symbolic simulation

Pankaj Chauhan, Edmund M. Clarke, Daniel Kroening

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(151.46 KB) Additional Information: full citation, abstract, references, index terms

Parametric representations used for symbolic simulation of circuits usually use BDDs. After a few steps of symbolic simulation, state set representation is converted from one parametric representation to another smaller representation, in a process called reparameterization. For large circuits, the reparametrization step often results in a blowup of BDDs and is expensive due to a large number of quantifications of input variables involved. Efficient SAT solvers have been applied successfully for ...

Keywords: SAT checkers, bounded model checking, parametric representation, safety property checking, symbolic simulation

19 Formal Verification of the Pentium® 4 Floating-Point Multiplier

R. Kaivola, N. Narasimhan

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(182.07 KB) Publisher Site Additional Information: full citation, abstract

We present the formal verification of the floating-point multiplier in the Intel IA-32 Pentium ™ microprocessor. The verification is based on a combination of theorem-proving and BDD based model-checking tasks performed in a unified hardware verification environment. The tasks are tightly integrated to accomplish complete verification of the multiplier hardware coupled with the rounder logic. The

f

approach does not rely on specialized representations like Binary Moment Diagrams or its variants.

20 Design for Verification at the Register Transfer Level

Indradeep Ghosh, Krishna Sekar, Vamsi Boppana

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(235.31 KB) Publisher Site Additional Information: full citation, abstract

In this paper we introduce a novel concept that can be used for augmenting simulation based verification at the Register Transfer Level (RTL). In this technique the designer of an RTL circuit introduces some well understood extra behavior (through some extra circuitry) into the circuit under verification. This can be termed as design for verification. During RTL simulation this extra behavior is utilized in conjunction with the original behavior to exercise the design more thoroughly thus making ...

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Terms used **symbolic trajectory evaluation** Found **31** of **142,346**

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21 On embedding a microarchitectural design language within Haskell

John Launchbury, Jeffrey R. Lewis, Byron Cook

September 1999 **ACM SIGPLAN Notices , Proceedings of the fourth ACM SIGPLAN international conference on Functional programming**, Volume 34 Issue 9

Full text available: pdf(1.26 MB) Additional Information: full citation, abstract, references, citings, index terms

Based on our experience with modelling and verifying microarchitectural designs within Haskell, this paper examines our use of Haskell as host for an embedded language. In particular, we highlight our use of Haskell's lazy lists, type classes, lazy state monad, and unsafe Perform IO, and point to several areas where Haskell could be improved in the future. We end with an example of a benefit gained by bringing the functional perspective to microarchitectural modelling.

22 Software integration: An example of linking formal methods with case tools: a model checker for statecharts

Nancy Day

October 1993 **Proceedings of the 1993 conference of the Centre for Advanced Studies on Collaborative research: software engineering - Volume 1**

Full text available: pdf(850.40 KB) Additional Information: full citation, abstract, references

Computer-Aided Software Engineering (CASE) tools encourage users to codify the requirements for the design of a system early in the development process. They often use graphical formalisms, simulation, and prototyping to help express ideas concisely and unambiguously. Some tools provide little more than syntax checking but others can test the model for reachability of conditions, nondeterminism, or deadlock. In this paper, we present an example of how commercial CASE tools can be linked with for ...

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23 Improved SAT-based Bounded Reachability Analysis

Malay K. Ganai, Adnan Aziz

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(319.34 KB) Publisher Site Additional Information: full citation, abstract

Symbolic simulation is widely used in logic verification. Previous approaches based on BDDs suffer from space outs, while SAT-based approaches have been found fairly robust. We propose a SAT-based symbolic simulation algorithm using a noncanonical two-input AND/INVERTER graph representation and on-the-fly reduction algorithm on such a graph representation. Unlike previous approaches where circuit is explicitly unrolled, we propagate the symbolic values represented using the simplified AND/INVERT ...

24 Formal verification: Handling special constructs in symbolic simulation

Alfred Kölbi, James Kukula, Kurt Antreich, Robert Damiano

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(109.20 KB) Additional Information: full citation, abstract, references, index terms

Symbolic simulation is a formal verification technique which combines the flexibility of conventional simulation with powerful symbolic methods. Some constructs, however, which are easy to handle in conventional simulation need special consideration in symbolic simulation. This paper discusses some special constructs that require unique treatment in symbolic simulation such as the symbolic representation of arrays, an efficient This paper discusses some special constructs that are unique to symb ...

Keywords: formal verification, symbolic simulation

25 Reliable verification using symbolic simulation with scalar values

Chris Wilson, David L. Dill

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(150.89 KB) Additional Information: full citation, abstract, references, index terms

This paper presents an algorithm for hardware verification that uses simulation and satisfiability checking techniques to determine the correctness of a symbolic test case on a circuit. The goal is to have coverage greater than that of random testing, but with the ease of use and predictability of directed testing. The user uses symbolic variables in simple directed tests to increase the input space that is explored. The algorithm, which is called quasi-symbolic simulation, ...

26 Formal hardware verification by integrating HOL and MDG

V. K. Pisini, S. Tahar, P. Curzon, O. Ait-Mohamed, X. Song

March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**

Full text available: pdf(625.19 KB) Additional Information: full citation, abstract, references, index terms

In order to overcome the limitations of automated tools and the cumbersome proof process of interactive theorem proving, we adopt a hybrid approach for formal hardware verification which uses the strengths of theorem proving (HOL) with powerful mathematical tools such as induction and abstraction, and the advantages of automated tools (MDG) which support equivalence checking and model checking. The MDG system is a decision diagram based verification tool, primarily designed for hardware ve ...

27 Exploiting positive equality and partial non-consistency in the formal verification of pipelined microprocessors

Miroslav N. Velev, Randal E. Bryant

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(39.23 KB) Additional Information: full citation, references, citings, index terms

28 Formally verifying a microprocessor using a simulation methodology

Derek L. Beatty, Randal E. Bryant

June 1994 **Proceedings of the 31st annual conference on Design automation**

Full text available: pdf(93.16 KB) Additional Information: full citation, references, citings, index terms

29 Symbolic Boolean manipulation with ordered binary-decision diagrams

Randal E. Bryant

September 1992 **ACM Computing Surveys (CSUR)**, Volume 24 Issue 3

Full text available: pdf(2.12 MB) Additional Information: full citation, abstract, references, citings, index terms

Ordered Binary-Decision Diagrams (OBDDs) represent Boolean functions as directed acyclic graphs. They form a canonical representation, making testing of functional properties such as satisfiability and equivalence straightforward. A number of operations on Boolean functions can be implemented as graph algorithms on OBDD data structures. Using OBDDs, a wide variety of problems can be solved through symbolic analysis. First, the possible variations in system parameters and op ...

Keywords: Boolean algebra, Boolean functions, binary-decision diagrams, branching programs, symbolic analysis, symbolic manipulation

30 Design verification and simulation: Improved symbolic simulation by functional-space decomposition

Tao Feng, Li-C. Wang, Kwang-Ting Cheng

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**

Full text available: pdf(195.34 KB) Additional Information: full citation, abstract, references

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This paper presents a functional-space decomposition approach to enhance the capability of symbolic simulation. In our symbolic simulator, the control part and data path of a circuit is separated, and their simulated results are recorded in different domains. A 2-tuple list structure is used to separate the results in the control and datapath domains. Then, the functional sub-space in the control domain can further be decomposed in order to achieve the optimal OBDD size and run time. We demonstr ...

31 Efficient Generation of Monitor Circuits for GSTE Assertion Graphs

Alan J. Hu, Jeremy Casas, Jin Yang

November 2003 **Proceedings of the 2003 International Conference on Computer-Aided Design (ICCAD'03) - Volume 00**

Full text available: Publisher Site Additional Information: full citation, abstract

Generalized symbolic trajectory evaluation (GSTE) is a powerful,new method for formal verification that combines the industrially-provenscalability and capacity of classical symbolic trajectoryevaluation with the expressive power of temporal-logic modelchecking. GSTE was originally developed at Intel and hasbeen used successfully on Intel's next-generation microprocessors.However, the supporting algorithms and tools for GSTE are stillrelatively immature.GSTE specifications are given as assertion ...

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Terms used **assertion graph**

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1 A data-driven model for a subset of logic programming

Lubomir Bic, Craig Lee

October 1987 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 9 Issue 4

Full text available: pdf(2.24 MB) Additional Information: full citation, abstract, references, citings, index terms, review

There is a direct correspondence between semantic networks and a subset of logic programs, restricted only to binary predicates. The advantage of the latter is that it can describe not only the nodes and arcs comprising a semantic net, but also the data-retrieval operations applied to such nets. The main objective of this paper is to present a data-driven model of computation that permits this subset of logic programs to be executed on a highly parallel computer architecture. We demonstrate ...

2 Execution of logic programs on a dataflow architecture

Lubomir Bic

January 1984 **ACM SIGARCH Computer Architecture News , Proceedings of the 11th annual international symposium on Computer architecture**, Volume 12 Issue 3

Full text available: pdf(623.20 KB) Additional Information: full citation, abstract, references, citings, index terms

Logic programming is a mathematical formalism capable of expressing certain classes of problems in a non-procedural manner. Furthermore, logic programs do not presuppose a von Neumann computer architecture and are therefore inherently well suited to parallel computations. In this paper we consider a data-driven model for interpreting logic programs and investigate the architectural requirements necessary to support its implementation. It will be shown that the model is capable of exploiting ...

3 GSTE through a case study

Jin Yang, Amit Goel

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(183.43 KB) Additional Information: full citation, abstract, references, citings, index terms

Generalized Symbolic Trajectory Evaluation (GSTE) [17, 18, 19] is a very significant extension of STE that has the power to verify all ω-regular properties but at the same time preserves the benefits of the original STE [16]. It also extends the symbolic quaternary model used by STE to support seamless model refinement for efficiency and accuracy trade-off in GSTE model checking. In this paper, we present a case study on FIFO verification to illustrate the strength of GSTE and demonstrate ...

4 Efficient Generation of Monitor Circuits for GSTE Assertion Graphs

Alan J. Hu, Jeremy Casas, Jin Yang

November 2003 **Proceedings of the 2003 International Conference on Computer-Aided Design (ICCAD'03) - Volume 00**

Full text available: Publisher Site Additional Information: full citation, abstract

Generalized symbolic trajectory evaluation (GSTE) is a powerful,new method for formal verification that combines the industrially-provenscalability and capacity of classical symbolic trajectoryevaluation with the expressive power of temporal-logic modelchecking. GSTE was originally developed at Intel and hasbeen used successfully on Intel's next-generation microprocessors.However, the supporting algorithms and tools for GSTE are stillrelatively immature.GSTE specifications are given as assertion ...

5 Real chalenges and solutions for validating system-on-chip: High level formal verification of next-generation microprocessors

Tom Schubert

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(249.00 KB) Additional Information: full citation, abstract, references, index terms

Formal property verification has been an effective complement to pre-silicon validation of several Intel Pentium 4 CPU designs at Intel Corporation. The principal objective of this program has been to prove design correctness rather than hunt for bugs. In the process, we have evolved our tools and methodology and are now applying FPV techniques to protocol level properties. Moving forward, new technologies such as GSTE and SAT offer the potential to significantly increase the scope of what can b ...

Keywords: formal property verification

6 Graph-based retrieval of information in hypertext systems

Yuri Quintana, Mohamed Kamel, Andrew Lo

November 1992 **Proceedings of the 10th annual international conference on Systems documentation**

Full text available: pdf(1.07 MB) Additional Information: full citation, references, citings, index terms

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[PPT] Symbolic Simulation 2002
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... Add fairness. "Generalized **Symbolic Trajectory** Evaluation". ... If check is X, then select some symbol to **strengthen**. As BDD variable, rather than as tagged X. ...
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... jin.yang, carl.seger @intel.com Abstract **Symbolic trajectory** evaluation (STE) is a lattice ... We further **strengthen** the power of GSTE by introducing a form of ...
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Mark Aagaard: Research
... need to **strengthen** the connection between the two techniques. This involves both mathematical reasoning about the semantics of **symbolic trajectory** evaluation ...
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... verification of the IM to the combi-nation of **symbolic trajectory** evaluation (STE ...
si will hold.In the final correctness statement (2), we **strengthen** Equation 1 ...
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[PPT] Lazy Symbolic Model Checking
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... Two Case Studies. STE : the Success Story. STE - **Symbolic Trajectory** Evaluation. ... Model Checking Normal Satisfiability. Phase 1: **strengthen** antecedents backward. ...
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... i:= i+1. Another way to **strengthen**. Invent a lemma, L(s) that we believe to hold in the reachable states. ... **Symbolic Trajectory** Evaluation (STE). a. b. c. d. ...
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[PS] ELECTRONIC WORKSHOPS IN COMPUTING Series edited by Professor CJ ...
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... 2.1 **Symbolic trajectory** evaluation STE is an automatic model checking algorithm originally proposed ... Now we take Result 2 and **strengthen** its antecedent using a ...
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... 12]), thus, after some symbolic manipulation, we can **strengthen** condition 3 of ... and the notion of com- pletion functions [5]. **Symbolic Trajectory** Evaluation (STE ...
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[PS] Appeared at FMCAD, November 2002, LNCS 2517, pp 1-18.
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... 2.3 **Symbolic Trajectory** Evaluation Circuit correctness in **symbolic trajectory** evaluation
is stated ... If we use the same indexingto **strengthen** the consequent, and ...
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... a property P is an invariant, we prove it is *inductive* % This is similar to Amir Pnueli's rule for Universal Invariance % Except we **strengthen** the actual ...
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... For example, **symbolic trajectory** evaluation carries out symbolic simulation of hardware in a ... with k-induction enriched with invariant **strengthen**- ing, whereas ...
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[PS] Digital Circuit Verification using
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... describe a technique for formal verfication, called **symbolic trajectory** evaluation that ... words, strengthening the circuit state can only **strengthen** the successor ...
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... In **Symbolic Trajectory** Evaluation (STE), the specifi- cation language consists of
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... a compositional model checker and a procedure for Generalized **Symbolic Trajectory** Evaluation. ... In particular, our framework allows us to **strengthen** a "suAEcient ...
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... **Symbolic Trajectory** Evaluation (STE) is a form of model checking fundamentally based
on ... Therefore, we could choose to **strengthen** the notion of graphp to ...
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... publications, periodicals, curricula and standards) to **strengthen** the society ... Systems" E. Thomas Schubert "Composing **Symbolic Trajectory** Evaluation Results" S ...
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Proof Planning for Automating Hardware. Verification. Francisco J. Cantu-Ortiz. TH. EU. NIVERS. IT. Y. O. F. EDI. NBU. RG. H. Ph.D. University of Edinburgh. 1997 ...
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[PS] Programming Research Group Model checking data-independent systems

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... 2.4.5 **Symbolic Trajectory** Evaluation **Symbolic Trajectory** Evaluation (STE) [SB95] is a model checking algorithm which com- bines abstraction together with ...
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... the termination of symbolic procedures for the **reachability analysis** of initialized ... We **strengthen** these results and give a uniform ... First, the **edge label**. 1. ^. ...
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... graph to generate a set of test cases, each test case being of the form (preamble(p) :: OP, postulate(N)), where OP is the **label** of an **edge** joining the ...
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... 2. Each **label** of anedge has four components: the ... the result of taking that **edge** is that ... **Reachability analysis** of pushdown automata: application to modelChecking ...
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... To the best of our knowl- **edge**, this property has not been exploited so ... the C-1-D Equivalence Check is conservative in cases where **reachability analysis** of the ...
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[PS] Specification and Test of Real-Time Systems
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... be found by reading the verdict **label** of the ... coverage criterion aims at executing every **edge** in the ... It will possibly also enable **reachability analysis** to be ...
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> [PS] Aalborg University Institute for Electronic Systems Department of ...
> File Format: Adobe PostScript - View as Text
> ... We will especially focus on the **reachability analysis**, since experiments by Lind-Nielsen et.al ... must be in the same partition, we add an **edge** between them in ...
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... we prove that the result of the function fixpoint indeed satisfies the dataflow inequations fixpoint.(s) ≥(transf n fixpoint.(n)) for every **edge** n → s in ...
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‰x7†'†, 'T?r? $, ¤ 6 contains an **edge** from 2 x0 ...
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... work in this area focusses on **reachability analysis**, rather than ... for each circuit node, and an **edge** for the ... is not isomorphic to any other structural **label**. ...
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> la- bel>$] where the first **label** represents the execution initiation ...
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... to the labelling algorithms used to **label** RG. ... a timed automaton, following which **reachability analysis** may be ... traversal: there exists a probabilistic **edge** (l; g ...
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... **edge** (within { }) are reset to the value 0; the values of all other clocks remain the same. We also note that conditions on the values of clocks which **label** ...
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... the inductive hypothesis. We propose several techniques that can automatically **strengthen** a given property. Keywords: embedded languages ...
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... 1Here, isomorphism means a **label**-preserving bijection ... m1 does notcontain any call **edge** labelled. ... **Reachability analysis** of pushdown automata: Application to model ...
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... 14:15. Plenary talk Ga'bor Herman (New York):Recovery of **Label** Distributions. ... However, traditional **reachability analysis** techniques can result in a state space ...
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... be checked syntactically and on-the-fly on the **label** of the ... we identify suAEcient conditions under which such a quantitative **reachability analysis** can always ...
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... This property is typically verified by performing a **reachability analysis** on a state-transition graph created ... A type acts as a generic class **label** for an entity ...
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[PS] The Theory of Timed I/O Automata Dilsun K. Kaynar, Nancy Lynch ...
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... of facilitating automated verification based on **reachability analysis** seems to ... By definition of the **edge** set of G, (fi. i. ... by an arrow annotated with a **label** a, b ...

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[PS] ISSN 1399-8145 AALBORG UNIVERSITY DEPARTMENT OF COMPUTER SCIENCE
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... It is our thesis that the symbolic techniques developed for **reachability analysis** of real ... An **edge** is labeled with one of three kinds of actions: The machine can ...
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[PS] REAL-TIME SYSTEM ANALYSIS BASED ON
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... For timed automaton model, we describe the **reachability analysis** approaches as follows. Alur et al. ... For an **edge** ed = (q. 1. ; a; q. 2. ... 2. and **label**(ed) = a. ...
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[PS] Techniques for the Construction and Analysis of
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... classical process algebra, providing facilities like model-checking, and **reachability analysis**. ... performance measures from SPA models would **strengthen** a weak ...
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> [PS] BRICS NS-95-2
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> ... action is already specified by an outgoing **edge**, nothing new ... is an inifinite **label** set ... Section 3, we give an introduction to the **reachability analysis** of linear ...
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[PS] ST eP STeP The Stanford Temporal Prover
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... have to (a) **strengthen** the original formula, or (b) first prove some ... program ::= f (decl j procedure) [;] g composite stmt [; **label**] procedure ::= procedure id ...
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[PS] AUTOMATIC ANALYSIS OF HYBRID SYSTEMS
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... The finite mutual simulation is sufficient for **reachability analysis** and thus ... controller automaton is required to traverse an **edge** with the same **label**. ...
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... be low between messages, and all messages must start witha bit 1. The first bit synchronizes the sender and receivers, all know that the first up-going **edge**. ...
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... Forward **reachability analysis**. . . . ... step (l, *) a)(l0, *0) occurs if there exists an **edge** e = hl ... with this timed automaton is {l0, l1} * R>=0, the **label** set is ...
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... the idea is, therefore, to **strengthen** the proof ... quite some work done on automated **reachability analysis** for communication ... is a triple M = (S, R, **Label**) where. ...
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... 124 5.7 Symbolic Formulation of **Reachability Analysis** . ... error process where one has to iteratively **strengthen** the invariant ... form ITE(F, T1, T2), we **label** F as ...
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... **Edge** labels (called. ... f leading to the denotation of y, without mentioning the **label** at the root of x; to assert the **label** at the root of x, there is alabelling ...
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... as deciding the truth of a temporal logic formula, performing **reachability analysis**, and state ... which has a vertex for each circuit node, and an **edge** for the ...
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... in Figure 6 (b). In general, we define a GSTE **assertion graph** as a ... edges, and ant and cons are functions that map each **edge** to an antecedent **label** and a ...
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... 2. i ; hb. 1. ; b. 2. i) j (a. 1. ; b. 1.) 2 E. 1. and (a. 2. ; b. 2.) 2 E. 2.
g : Edges in G are labeled with the corresponding **edge-label** pair. If G. 1. and
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... of a path if a is in the **label** of the ... In general, an **assertion graph** is a directed graph with a distinguished ... Each **edge** e is labeled with an antecedent ant(e ...
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